United States Patent No. 6,153,494 to Hsieh, et al., entitled "Method to increase the coupling ratio of word line to floating gate by lateral coupling in stacked-gate flash" and filed on ~~February 11, 1998~~ May 12, 1999. The object of this invention is to provide a method of forming a stacked-gate flash memory having a shallow trench isolation with a high-step in order to increase the lateral coupling between the word line and the floating gate. Hsieh disclosed a step of forming nitride layer and then forming ~~hallow~~ shallow trench isolation (STI) through the nitride layer into the substrate. Then, oxide is filled into the STI, the nitride is then removed leaving behind a deep opening about the filled STI. The detailed description may refer to the prior art. A stacked-gate flash memory cell is provided having a shallow trench isolation with a high-step of oxide and high lateral coupling.

Please amend page 7 beginning line 2 with the following:

The present invention proposes a novel structure and method to fabricate the flash memory. The stacked-gate flash memory cell includes a trench formed in a substrate 2, please refer to FIGURE 4. A tunneling oxide 4 is formed on the surface of the substrate 2 and adjacent to the trench 4. A first part of the floating gate 6 is formed on the tunneling gate oxide 4. a raised (protruding) isolation filler 10 is formed in the trench and protruding over the upper surface of the first part of the floating gate 6, thereby forming a cavity 9 between the two adjacent raised isolation filler 10. A second part of the floating gate 12 is formed along the surface of the cavity to have a U-shaped structure in cross sectional view. The high level of the U-shaped structure is the same with the one of the raised isolation filler 10. a dielectric layer 14 is conformally formed on the surface of the second part of the floating gate 12 and a control gate 16 is formed on the

dielectric layer 14.

Please amend page 9, beginning line 2 with the following:

Next, turning to FIGURE 3, a portion of the polysilicon layer 6 is removed to form raised (protruding) isolation filler 10 that protruding over the etched surface the polysilicon 6, thereby forming cavity 9 between the raised isolation fillers 10. A high selectivity etching between oxide and polysilicon is utilized to this step. The step high of the raised isolation filler 10 can be controlled by the etching depth, namely the amount of the removal of the polysilicon. Next, a thin conductive layer 12 such as in-situ doped polysilicon ~~14~~ along the surface of the cavity 9 and the raised (protruding) isolation filler 10. The thickness of the thin conductive layer is about 100-1000 angstroms. Next, the thin conductive layer 12 is removed to expose the upper surface of the raised isolation filler 10 by CMP. The thin polysilicon layer 12 only remains on side wall and bottom of the cavity 9, as shown in FIGURE 4.

Please amend page 9, paragraph 2 beginning line 13 with the following:

The polysilicon layer 6 and the remained thin polysilicon layer ~~14~~ 12 serve as a floating gate and isolated by the raised isolation filler 10. As another key feature of the present invention, remained thin polysilicon layer ~~14~~ 12 is conformally formed so as to follow the contours of the cavity 9, thus providing additional surface to the control gate dielectric that to be formed later. In another words, the polysilicon layer 12 should not be filled the totally the cavity 9.

**Amendments to the Claims:**